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Activation-aware Slack Assignment (ASA) for Mode-wise Power Saving in High-End ISP

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Outline

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3. Key Idea
4. Design Flow
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Power consumption is the most competitive factor in recent mobile SoC.

We have to pursue the highest power efficiency in both design and field.

Design

Low power design technique
- Multi Vth and Leak Optimization
- Clock Gating
- Power Gating, etc…

Activation-aware Slack Assignment (ASA)

Field Usage

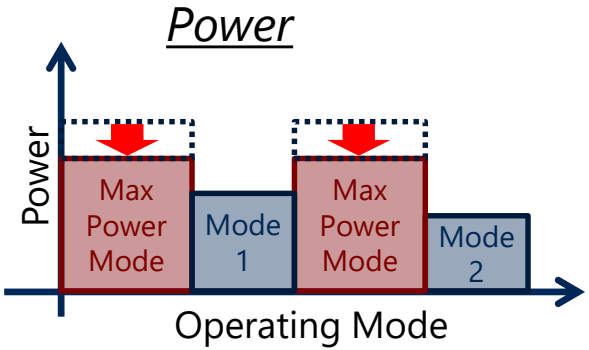
Adaptive Voltage Scaling (AVS) by
- Process
- Temperature
- Precision, etc…

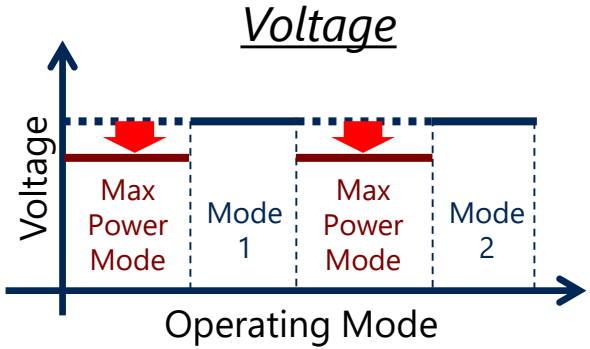
Operating Mode (Mode-wise AVS)

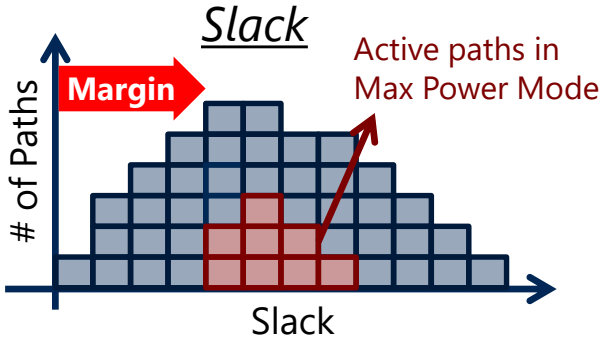
Motivation (Operating Mode)

In field usage, power consumption changes depending on the operating mode

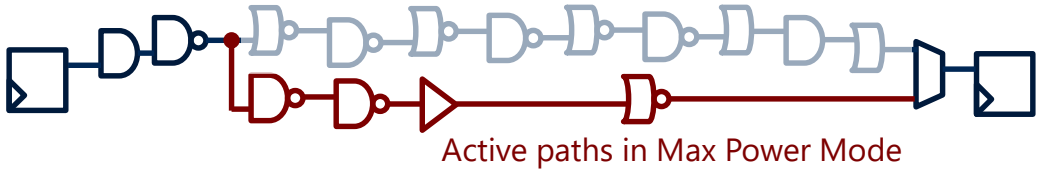
In design phase, timing of all the physically existing paths are verified at fixed voltage corners







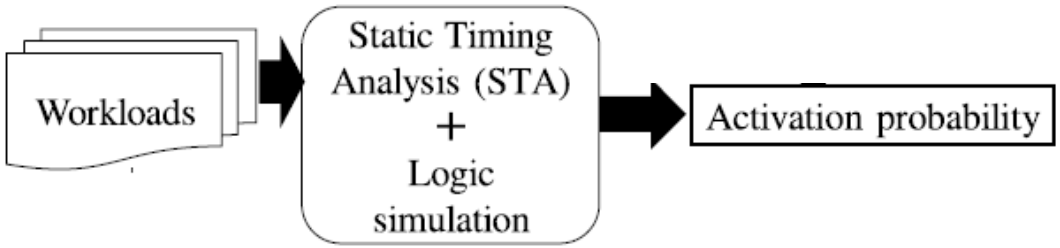
There is ***timing margin*** that can be used for ***voltage lowering*** with the same performance.

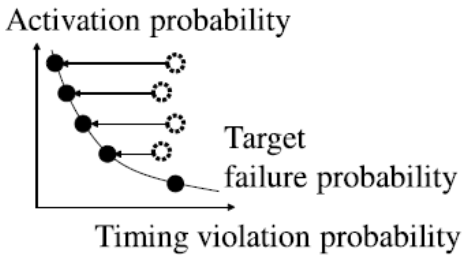


If the critical paths in STA are not activated in maximum power consumption mode (Max Power Mode)

Motivation (Activation-aware Slack Assignment)

Previous Work*





Assign slack to ***active*** paths extracted *in* ***all workloads***

Logic sim. in all workloads
Slack Assignment to active paths
} *involve long TAT for industrial design*

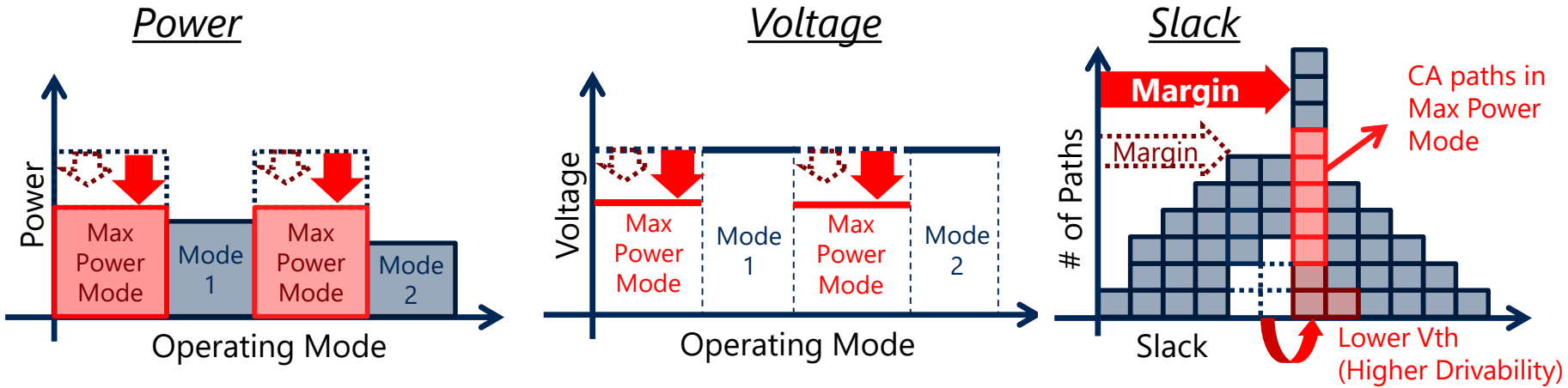
Assign slack to ***Critical-Active paths*** extracted in ***only Max Power Mode***
(CA paths)

*Y. Masuda, *et al.*, "Activation-Aware Slack Assignment for Time-to-Failure Extension and Power Saving," *IEEE Trans. On Very Large Scale Integration (VLSI) Systems*, vol. 26, no. 11, pp. 2217-2229, Aug. 2018 .

Key Idea

Mode-wise AVS + Activation-aware Slack Assignment (ASA)

Mode-wise ASA

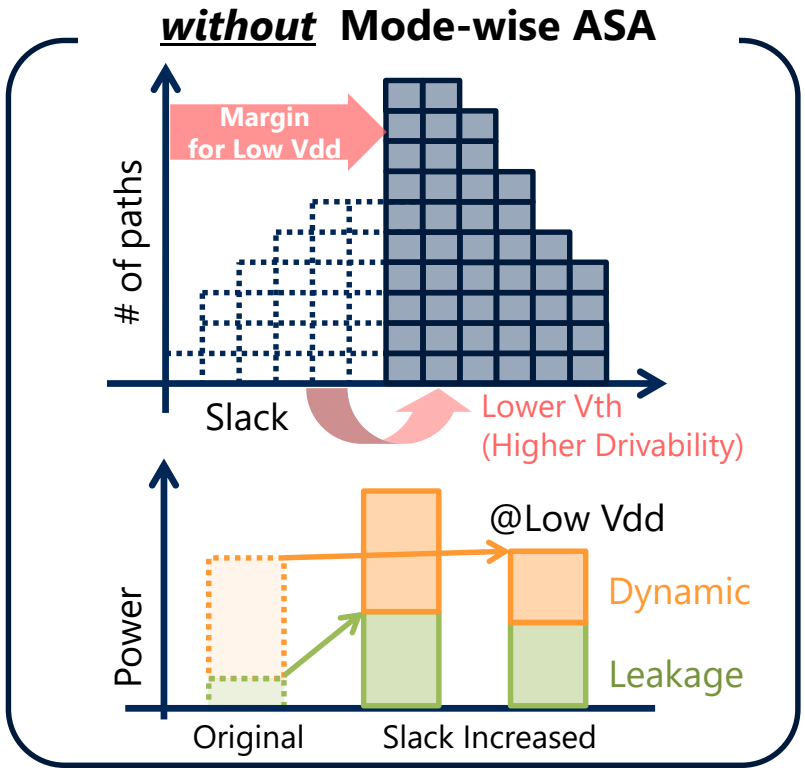


Mode-wise ASA can reduce the power more than Mode-wise AVS

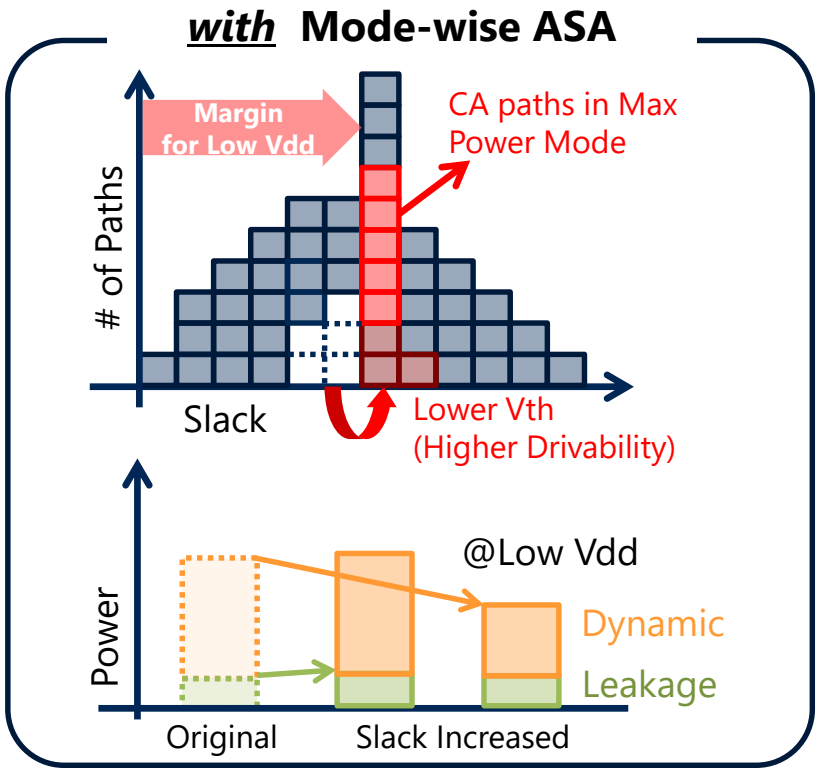
Increase slack for only **Critical-Active paths**

Key Idea (Mode-wise ASA)

CA Paths : Critical-Active Paths

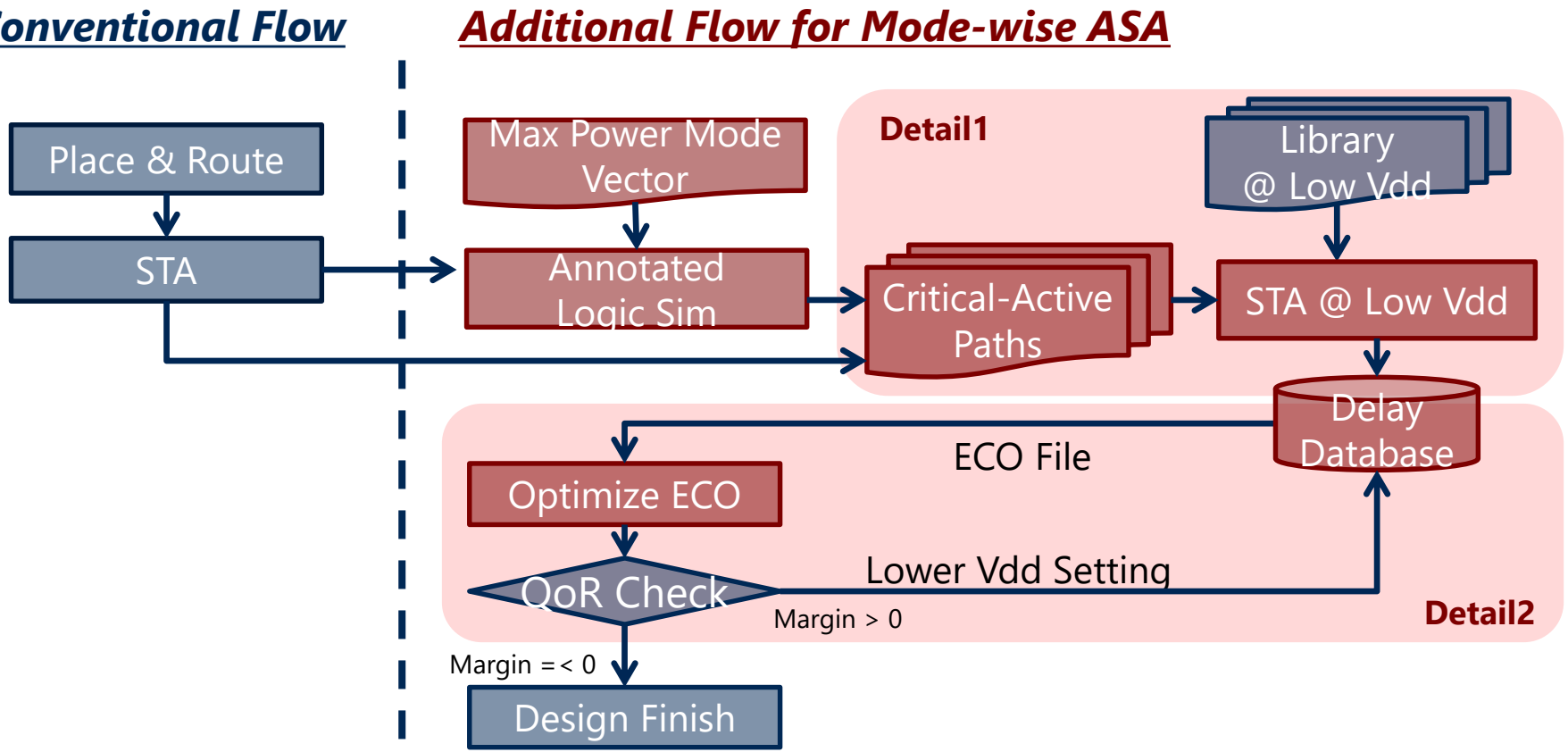


Leakage power increases ***significantly***
Total power at low vdd ***may not decrease***

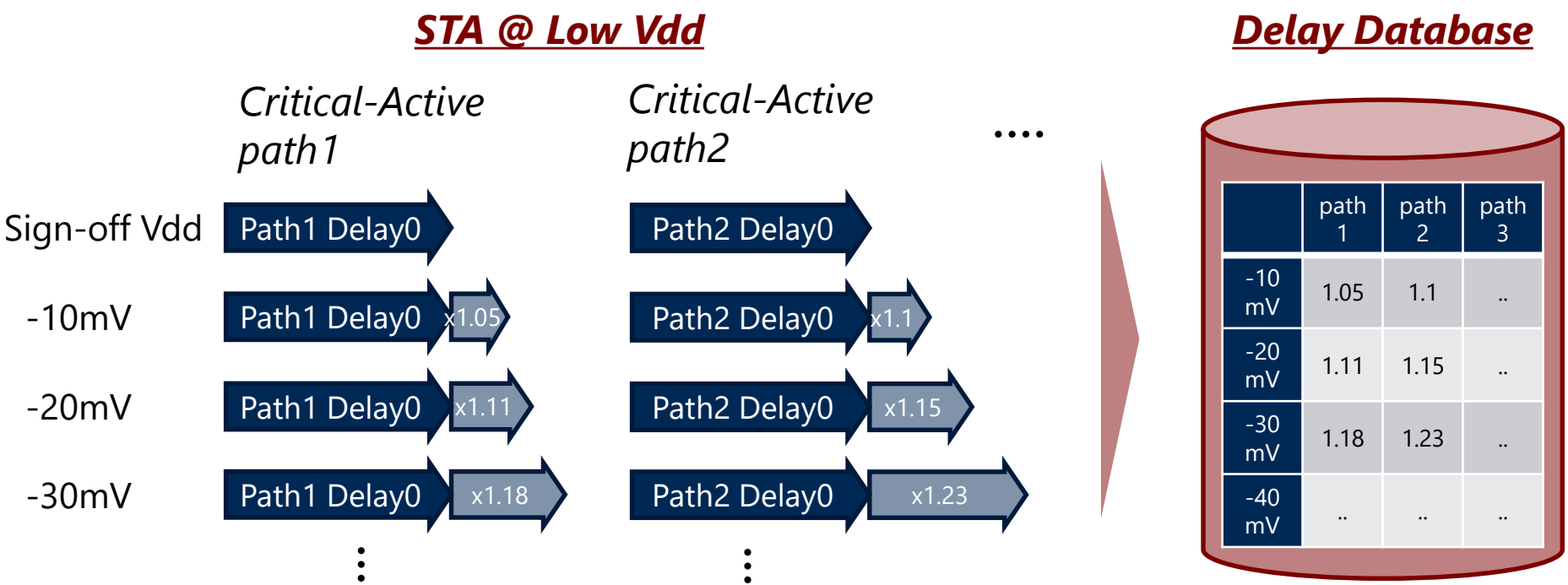


Leakage power only increases ***slightly***
Total power at low vdd ***decreases***

Design Flow

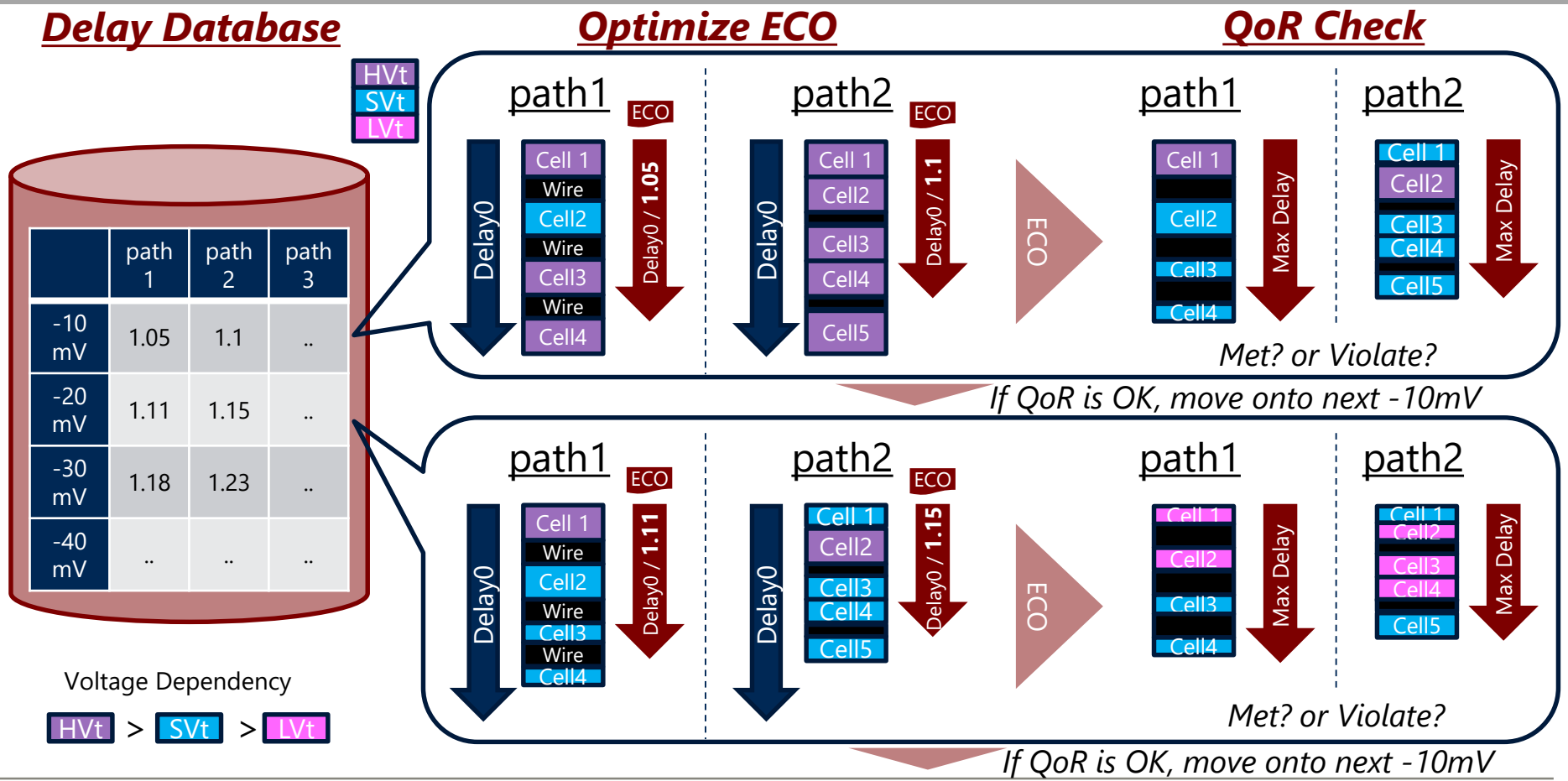

Conventional Flow
Additional Flow for Mode-wise ASA
Place & Route
STA
Max Power Mode Vector
Annotated Logic Sim
Detail1
Library @ Low Vdd
Critical-Active Paths
STA @ Low Vdd
Delay Database
ECO File
Optimize ECO
QoR Check
Lower Vdd Setting
Margin > 0
Detail2
Margin =< 0
Design Finish

Additional Flow (Detail 1)



Create a database of the delay increase when lowering the voltage for each CA paths

Additional Flow (Detail 2)

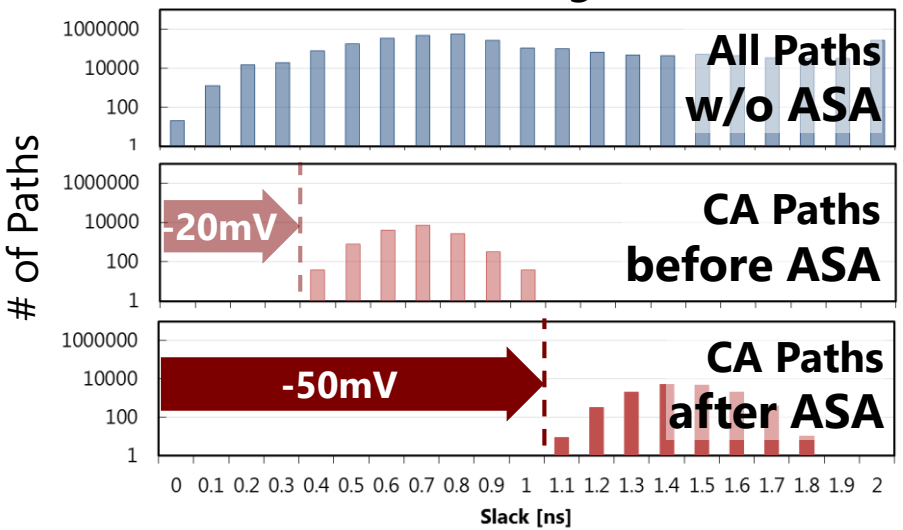


Evidence

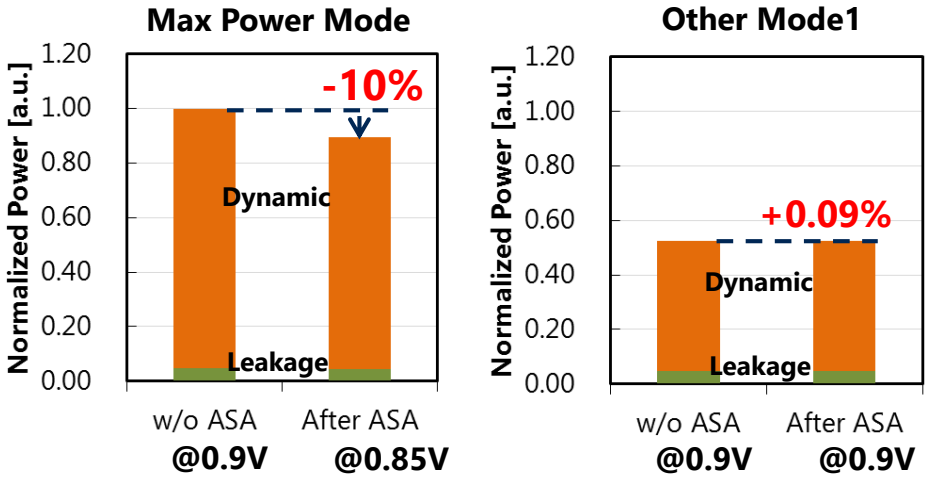
CA Paths : Critical-Active Paths

Mode-wise ASA → **Socionext's design High-end ISP**

Slack histogram



Power of each mode



✓ ASA enhance from -20mV to **-50mV**

✓ ASA save power by **10%** in Max Power Mode

Evidence (continued)

Design Info.

Func.	High-End ISP
Tech Node	28nm
Logic Gate	12.4M gates
Cell set	Low Vth, Standard Vth, High Vth

Mode-wise ASA effects

Mode	Power				Area	Additional TAT
	Vdd Reduction	Dynamic	Leakage	Total		
Max Power Mode	**50mV**	**-11%**	**-5%**	**-10%**	**+0.1%**	**1week**
Other Mode	**0mV**	**0%**	**+0.9%**	**+0.09%**		

- ✓ Changing to high drivability cell increase area by 0.1%
- ✓ Applying additional flow extends the design TAT by 1 week

Summary

- We propose mode-wise ASA compatible with industrial design
- The proposed ASA tunes the slack of only Critical-Active paths in Max Power Mode
- A case study shows that power is reduced by ***10%*** with ***50mV*** Vdd reduction
- Performance degradation and area penalties are negligibly small

Mode-wise ASA (Activation-aware Slack Assignment) effects

Mode	Power				Area	Additional TAT
	Vdd Reduction	Dynamic	Leakage	Total		
Max Power Mode	50mV	-11%	-5%	-10%	+0.1%	1week
Other Mode	0mV	0%	+0.9%	+0.09%		